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EXAMINER	
YANG, NELSON C	
ART UNIT	**PAPER NUMBER**
1641	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/177,814	GILTON, TERRY L.	
	Examiner	Art Unit	
	Nelson Yang	1641	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-29, 111, 112* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment of claims 1, 3-11, 13-29 is acknowledged and has been entered.

2. Applicant's addition of claims 111-112 is acknowledged and has been entered.

3. Claims 1, 3-11, 13-29, 111, 112 are currently pending.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Support could not be found for the limitation that the porous regions comprised the same material as the substrate. The only porous material the disclosure appears to discuss is porous silicon.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 3, 4, 7, 11, 18, 22-24, 111, 112 are rejected under 35 U.S.C. 102(e) as being anticipated by Northrup et al [US 5,882,496].

With respect to claim 1, Northrup et al teach an embodiment of a porous silicon electrophoresis device comprising a silicon member in which a plurality of spaced members or columns of porous silicon are formed (column 7, lines 38-43). A negative electrode is formed at one (inlet) end of porous silicon members or columns and a positive electrode is formed at an opposite (outlet) end of porous silicon members or columns (column 7, lines 43-50). Northrup et al further teach that the porous silicon members define an interface between two analysis devices (detectors), such as a PCR or an electrophoresis device (claims 11-12).

8. With respect to claim 3, Northrup et al teach that the columns have pore size of about 1 μm down to about 10 nm (column 7, lines 35-38). Therefore, the columns would be capable of functioning as capillary columns.

9. With respect to claim 4, the columns linearly traverse the substrate (figs. 7-8).

10. With respect to claim 7, the porous silicon can be used to increase the surface area of heated reaction chambers (column 2, lines 10-15).

11. With respect to claim 11, the reaction chambers constitute the entire porous silicon area (column 7, lines 15-36).

12. With respect to claims 18, 22-24, a negative electrode is formed at one (inlet) end of porous silicon members or columns and a positive electrode is formed at an opposite (outlet) end of porous silicon members or columns (column 7, lines 43-50). The electrodes act as a electrophoresis device (column 7, lines 37-50).

13. With respect to claims 111-112, Northrup et al teach the device comprises a silicon member (column 7, lines 38-43).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 5, 7, 8, 10, 11, 14, 25-29, 111, 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knoll [US 5,393,401] in view of Northrup et al [US 5,882,496].

With respect to claim 1, Knoll teaches a sensor comprising a silicon substrate (column 2, lines 60-62) with ion selective field effect transistors (column 4, lines 35-40) and ion-selective membranes (porous regions) formed in containments on the silicon substrate (column 5, lines 4-15). Knoll does not teach that the ion selective membranes are comprised of porous silicon.

Nothrup et al, however, teach the use of porous silicon membranes (column 3, lines 50-52), and further teach that porous silicon is capable of increasing the surface area of a silicon device for use in specific pore size arrays, and biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

Therefore, it would have been obvious to one of ordinary skill in the art for the ion selective membranes of Knoll to be comprised of porous silicon, as suggested by Nothrup et al, in order to increase the surface area of a silicon device for use in specific pore size arrays and

biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

16. With respect to claim 5, ion-selective membranes are formed in containments on the silicon substrate (column 5, lines 4-15), and therefore would only extend partially across the substrate.

17. With respect to claims 7, 8, 10-11, 25-28, Knoll teaches that the enzymes, antibodies microbes or organelles can be immobilized in the membrane (column 5, lines 9-15). Therefore the distance between the reaction regions and the end of the porous regions would be the same.

18. With respect to claim 14, Knoll teaches a sensor comprising a silicon substrate (column 2, lines 60-62) with ion selective field effect transistors (column 4, lines 35-40).

19. With respect to claim 15, the FETs would have a voltage application component and a current detection component (column 4, lines 35-40).

20. With respect to claim 29, Knoll teaches that the ion-selective membranes can be protected by another layer of material (column 5, lines 4-9).

21. With respect to claims 111-112, Knoll teaches a sensor comprising a silicon substrate (column 2, lines 60-62)

22. Claims 1, 3, 5, 6-11, 14, 15, 18, 22-24, 111, 112 are rejected under 35 U.S.C. 102(b) as being anticipated by Heller et al [US 5,605,662] in light of Vickers et al [US 5,693,946], in view of Northrup et al [US 5,882,496].

With respect to claim 1, Heller et al teach a device comprising a silicon wafer (column 12, lines 46-52) having a matrix of addressable microscopic locations on its surface, where each individual micro-location is able to electronically control and direct the transport and attachment

of specific binding entities to itself (column 5, lines 35-43). Each micro-location comprises a permeation layer, an attachment layer, and a binding entity layer (fig. 2, column 10, lines 59-67). The permeation and attachment layers are porous (column 15, lines 1-6). Detection may be performed by CCD detectors associated directly with the device in a sandwich arrangement (column 20, lines 45-50). One of ordinary skill in the art would realize that CCD detectors comprise FETs, as evidenced by Vickers et al (column 4, lines 1-10). Heller et al do not teach that the porous layers comprise the same material as the substrate, silicon.

Nothrup et al, however, teach the use of porous silicon membranes (column 3, lines 50-52), and further teach that porous silicon is capable of increasing the surface area of a silicon device for use in specific pore size arrays, and biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

Therefore, it would have been obvious to one of ordinary skill in the art for the layers of Heller et al to be comprised of porous silicon, as suggested by Nothrup et al, in order to increase the surface area of a silicon device for use in specific pore size arrays and biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

23. With respect to claim 3, the microlocation are part of microcapillaries (column 24, lines 15-20).

24. With respect to claim 5, the permeation layer constitutes only part of each microlocation (fig. 6), and therefore would only extend partially across the substrate.

25. With respect to claim 6, microlocations were used for negative control for nonspecific binding (column 25, lines 1-5), which would render these microlocations as control columns.

26. With respect to claims 7-11, the binding entity layers are located underneath the permeation and attachment layers, and may contain antibodies (fig. 6, column 11, lines 15-40).

27. With respect to claim 14, detection may be performed by CCD detectors associated directly with the device in a sandwich arrangement (column 20, lines 45-50). One of ordinary skill in the art would realize that CCD detectors comprise FETs, as evidenced by Vickers et al (column 4, lines 1-10).

28. With respect to claim 15, the FETs would have a voltage application component and a current detection component, as evidenced by Vickers et al (column 6, lines 9-25).

29. With respect to claims 18, 22-24, the device comprises microelectrodes located at the ends of the permeation layers (fig. 6), and the opposite charge of the specific binding entities can be applied to a specified microelectrode while the other microelectrodes are maintained at the sample charge (column 15, lines 55-65), resulting electrodes that are anodes or cathodes.

30. With respect to claims 111-112, Heller et al teach a device comprising a silicon wafer (column 12, lines 46-52).

31. Claims 1, 3-5, 7-9, 13, 16-20, 22-27, 111, 112 are rejected under 35 U.S.C. 102(e) as being anticipated by Burns et al [US 6,379,929] in view of Northrup et al [US 5,882,496].

With respect to claim 1, Burns et al teach a device with isothermally regulated reaction chambers (column 3, lines 45-50) and porous columns of micromachined channels for gel electrophoresis (column 57, lines 33-44) etched on silicon chips (column 57, lines 22-38) as well

as temperature sensors (column 62, lines 15-20). Burns et al do not teach that the porous columns are comprised of the same material as the silicon chip, porous silicon.

Nothrup et al, however, teach the use of porous silicon membranes (column 3, lines 50-52), and further teach that porous silicon is capable of increasing the surface area of a silicon device for use in specific pore size arrays, and biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

Therefore, it would have been obvious to one of ordinary skill in the art for the porous columns of Burns et al to be comprised of porous silicon, as suggested by Nothrup et al, in order to increase the surface area of a silicon device for use in specific pore size arrays and biological/chemical filters, while maintaining the capability of modification, such as being doped or coated using conventional integrated circuit and micromachining techniques.

32. With respect to claim 3, the channels are capable of capillary gel electrophoresis (column 57, lines 45-50), and therefore would be capillary columns.

33. With respect to claims 4, 5, the channels linearly traverse the chip, but only extend partially across the substrate (fig. 2b).

34. With respect to claims 7-9, 25-27, Burns et al teach that following separation of amplification products, a probe conjugated to an antibody may be brought into contact with the amplified marker sequence (column 53, lines 30-40).

35. With respect to claim 13, Burns et al teach that the silicon chip comprise temperature sensors (column 62, lines 15-20).

36. With respect to claim 16, a microprocessor may be on-wafer (column 32, lines 45-52).

37. With respect to claim 17, the output information is stored by the microprocessor (column 32, lines 45-52). The microprocessor would thus act as a memory device.

38. With respect to claims 18-20, Burns et al teach that the device comprises a migration facilitator such as a pump (column 35, lines 50-55), and sealed valves for flow control (column 44, lines 9-40).

39. With respect to claims 22-24, electrodes are located at either end of the channels (column 31, lines 55-65) for purposes of electrophoresis (column 32, lines 65-67), which would require electrodes at one end of the channels to be anodes, and electrodes at the other end to be cathodes.

40. With respect to claim 111-112, Burns et al teach silicon chips (column 57, lines 22-38).

41. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al [US 6,379,929]] in view of Northrup et al [US 5,882,496], and further in view of Dubrow [US 5,948,227].

Burns et al teach a device with isothermally regulated reaction chambers (column 3, lines 45-50) and porous gel columns of micromachined channels for gel electrophoresis (column 57, lines 33-44) etched on silicon chips (column 57, lines 22-38) as well as temperature sensors (column 62, lines 15-20). Burns further teach that the device comprises a migration facilitator such as a pump (column 35, lines 50-55), and sealed valves for flow control (column 44, lines 9-40). Burns et al fail to teach that the migration facilitator comprises a vacuum source.

Dubrow, however, teaches a vacuum source (column 7, lines 1-10) and further teaches that the vacuum source allows a solution to be driven into a capillary channel (column 7, lines 1-10).

Therefore it would have been obvious to one of ordinary skill in the art to have a vacuum source in the device of Burns et al and Nothrup et al, as suggested by Dubrow, in order to drive a solution into the capillary channels.

Response to Arguments

42. Applicant's arguments with respect to claims 1, 3-11, 13-29, 111, 112 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

43. No claims are allowed.

44. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

45. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Yang whose telephone number is (571) 272-0826. The examiner can normally be reached on 8:30-5:00.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Long V. Le can be reached on (571)272-0823. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Yang
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